WHAT IS CLAIMED IS:

1. A memory device comprising:

a semiconductor substrate;

a first gate insulator on a first portion of a semiconductor substrate;

a storage node on the first gate insulator;

a tunnel junction barrier on the storage node;

a data electrode on the tunnel junction barrier;

a second gate insulator layer on a sidewall of the tunnel junction barrier;

a third gate insulator on a second portion of the substrate adjacent the tunnel junction barrier;

a gate electrode on the second gate insulator and the third gate insulator; and

first and second impurity-doped regions in the substrate coupled by a channel through the first and second portions of the substrate.

2. A memory device according to Claim 1, wherein the storage node is on a first channel in the first portion of the substrate, and wherein the gate electrode is on a second channel in the second portion of the substrate that couples the first channel to the first impurity-doped region.

3. A memory device according to Claim 2, wherein the second channel is configured to serve as a source/drain for the first channel.

4. A memory device according to Claim 1, further comprising a fourth gate insulator on a second sidewall of the tunnel junction barrier and a fifth gate insulator on a third portion of the substrate between the tunnel junction barrier and the second impurity-doped region, and wherein the gate electrode is disposed on the fourth and fifth gate insulators.

5. A memory device according to Claim 4, wherein the gate electrode is on a third channel region in the third portion of the substrate that couples the first channel to the second impurity-doped region.

6. A memory device according to Claim 5, wherein the third channel is configured to serve as a source/drain for the first channel.

7. A memory device according to Claim 4, wherein the second, third, fourth and fifth gate insulators comprise respective portions of a continuous insulation layer conforming to a top of the data electrode and to the sidewalls of the tunnel junction barrier and to surfaces of the substrate adjacent thereto, and wherein the gate electrode comprises a continuous conductive layer overlying the continuous insulation layer.

8. A memory device according to Claim 7, wherein the gate electrode further comprises conductive sidewall spacers interposed between the portions of the second insulation layer on the sidewalls of the tunnel junction barrier and the continuous conductive layer.

9. A memory device according to Claim 1, wherein the second and third gate insulators comprise respective portions of a continuous insulation layer conforming to the sidewall of the tunnel junction barrier and to a surface of the second portion of the substrate, and wherein the gate electrode comprises a continuous conductive layer overlying the continuous insulation layer.

10. A memory device according to Claim 9, wherein the gate electrode further comprises a conductive sidewall spacer interposed between the portion of the second insulation layer on the sidewall of the tunnel junction barrier and the continuous conductive layer.

11. A memory device according to Claim 10, further comprising an insulation layer on the data electrode, and wherein the gate electrode comprises a portion on the insulation layer on the data electrode.

12. A memory device according to Claim 10, wherein the gate electrode comprises a continuous conductive layer overlying the second and third gate insulators and the data electrode.

13. A memory device, comprising:

a semiconductor substrate;

a tunnel junction barrier transistor having a storage node on the substrate, a tunnel junction barrier on the storage node, and a gate electrode on a sidewall of the tunnel junction barrier that controls a channel of the tunnel junction barrier transistor;

a first planar transistor having a first channel in the substrate disposed transverse to the channel of the tunnel junction barrier transistor and controlled by the storage node of the tunnel junction barrier transistor; and

a second planar transistor having a second channel in the substrate disposed adjacent to the first planar transistor and transverse to the channel of the tunnel junction barrier transistor and having a gate electrode electrically coupled to the gate electrode of the tunnel junction barrier transistor.

14. A memory device according to Claim 13, wherein the gate electrodes of the tunnel junction barrier transistor and the second planar transistor comprise a continuous conductive layer having a first portion on the sidewall of the tunnel junction barrier and a second portion that extends transverse to the first portion onto the channel of the second planar transistor.

15. A memory device according to Claim 13, wherein the second planar transistor comprises second channels on respective sides of the first channel.

16. A memory device according to Claim 15, wherein the gate electrodes of the tunnel junction barrier transistor and the second planar transistor comprise a first continuous conductive layer having a first portion on a first sidewall of the tunnel junction barrier and a second portion that extends transverse to the first portion onto a first one of the second channels of the second planar transistor, and a second continuous conductive layer having a first portion on a second sidewall of the tunnel junction barrier opposite the first sidewall and a second portion that extends transverse to the first portion onto a second one of the second channels of the second planar transistor.

17. A memory device according to Claim 15, wherein the gate electrodes of the tunnel junction barrier transistor and the second planar transistor comprise a continuous conductive layer disposed on first and second opposing sidewalls of the

tunnel junction barrier and on respective portions of the substrate adjacent the first and second sidewalls.

18. A memory device according to Claim 15, further comprising respective first and second impurity doped regions in the substrate on respective sides of the tunnel junction barrier transistor and electrically coupled to respective ones of the second channels.

19. A method of forming a memory device, the method comprising:

forming a multiple layer pattern including a first gate insulator on a first portion of a semiconductor substrate, a storage node on the first gate insulator, a tunnel junction barrier on the storage node and a data electrode on the tunnel junction barrier;

forming a second gate insulator layer on a sidewall of the tunnel junction barrier and a third gate insulator on a second portion of the substrate adjacent the multiple layer pattern;

forming a gate electrode on the second and third gate insulators; and

forming first and second impurity-doped regions in the substrate coupled by a channel through the first and second portions of the substrate.

20. A method according to Claim 19, wherein the channel comprises a first channel controlled by the storage node and a second channel controlled by a portion of the gate electrode on the second portion of the substrate.

21. A method according to Claim 20, wherein the second channel is configured to serve as a source/drain for the first channel.

22. A method according to Claim 19:

wherein forming a second gate insulator layer on a sidewall of the tunnel junction barrier and a third gate insulator on a second portion of the substrate adjacent the multiple layer pattern comprises forming a continuous insulation layer on the data electrode, sidewalls of the multiple layer pattern, the second portion of the substrate and a third portion of the substrate on an opposite side of the multiple layer pattern;

wherein forming a gate electrode comprises forming respective conductive sidewall spacers on respective ones of the sidewalls of the multiple layer pattern and forming a continuous conductive layer on a portion of the continuous insulation layer on the data electrode, the conductive sidewall spacers and portions of the continuous insulation layer on the second and third portions of the substrate;

wherein the channel comprises a first channel controlled by the storage node and second and third channels controlled by respective portions of the continuous conductive layer on the second and third portions of the substrate; and

wherein the second and third channels are configured to electrically couple the first channel to respective ones of the first and second impurity doped regions.

23. A method according to Claim 19:

wherein forming a second gate insulator layer on a sidewall of the tunnel junction barrier and a third gate insulator on a second portion of the substrate adjacent the multiple layer pattern comprises forming a first continuous insulation layer on a first sidewall of the multiple layer pattern and on the second portion of the substrate and forming a second continuous insulation layer on a second sidewall of the multiple layer pattern and a third portion of the substrate adjacent thereto;

wherein forming a gate electrode comprises forming respective first and second conductive sidewall spacers on respective ones of the first and second sidewalls of the multiple layer pattern, forming a first continuous conductive layer on the first conductive sidewall spacer and a portion of the first continuous insulation layer on the second portions of the substrate, and forming a second continuous conductive layer on the second conductive sidewall spacer and a portion of the second continuous insulation layer on the third portion of the substrate;

wherein the channel comprises a first channel controlled by the storage node and second and third channels controlled by respective portions of the first and second continuous conductive layers on the second and third portions of the substrate; and

wherein the second and third channels are configured to electrically couple the first channel to respective ones of the first and second impurity doped regions.

24. A method according to Claim 19, wherein forming a multiple layer pattern comprises:

forming a first gate insulation layer on the substrate;

forming a first conductive layer on the first gate insulation layer;

forming alternating semiconductor and tunnel insulation layers on the first conductive layer;

forming a second conductive layer on the alternating semiconductor and tunnel insulation layers;

forming a first mask layer on the second conductive layer;

patterning the first gate insulation layer, the first conductive layer, the alternating semiconductor and tunnel insulation layers, the second conductive layer and the first mask layer to form first and second spaced apart trenches;

forming first and second insulation regions in respective ones of the first and second trenches;

removing a portion of the first mask layer to expose a portion of the second conductive layer between the first and second insulation regions;

forming a third conductive layer on the exposed portion of the second conductive layer;

forming a second mask layer on the third conductive layer; and

patterning the first gate insulation layer, the first conductive layer, the alternating semiconductor and tunnel insulation layers, the second conductive layer, the third conductive layer and the second mask layer to form the first gate insulator, the storage node, the tunnel junction barrier, the data electrode, and a mask pattern on the data electrode.

25. A method according to Claim 24, wherein forming a second gate insulator layer on a sidewall of the tunnel junction barrier and a third gate insulator on a second portion of the substrate adjacent the multiple layer pattern comprises forming a second gate insulation layer on the multiple layer pattern and adjacent portions of the substrate.

26. A method according to Claim 25, wherein forming a gate electrode comprises:

forming first and second conductive sidewall spacers on portions of the second gate insulation layer on first and second sidewalls of the multiple layer pattern;

forming a fourth conductive layer conforming to the first and second conductive sidewall spacers and the second gate insulation layer; and

patterning the fourth conductive layer to form a gate electrode on the multiple layer pattern, the first and second conductive sidewall spacers, and respective portions of the gate insulation layer adjacent the first and second conductive sidewall spacers.

27. A method according to Claim 26, wherein the conductive sidewall spacers and one or more semiconductor layers of the alternating semiconductor and tunnel insulation layers comprise silicon doped with impurities of a first conductivity type.

28. A method according to Claim 27, wherein the first conductive layer, the second conductive layer, and the fourth conductive layer comprise silicon doped with impurities of a second conductivity type.

29. A method according to Claim 26, wherein forming first and second impurity-doped regions in the substrate comprises implanting ions into the substrate using the gate electrode as an implantation mask.

30. A method according to Claim 19, wherein forming a multiple layer pattern comprises:

forming a first gate insulation layer on the substrate;

forming a first conductive layer on the first gate insulation layer;

forming alternating semiconductor and tunnel insulation layers on the first conductive layer;

forming a second conductive layer on the alternating semiconductor and tunnel insulation layers;

forming a first mask layer on the second conductive layer; and

patterning the first gate insulation layer, the first conductive layer, the alternating semiconductor and tunnel insulation layers, the second conductive layer and the first mask layer to form the multiple layer pattern and a mask pattern thereon.

31. A method according to Claim 30, wherein forming a second gate insulator layer on a sidewall of the tunnel junction barrier and a third gate insulator on a second portion of the substrate adjacent the multiple layer pattern comprises

forming a second gate insulation layer on the multiple layer pattern and adjacent portions of the substrate.

32. A method according to Claim 31, wherein forming a gate electrode comprises:

forming first and second conductive sidewall spacers on portions of the second gate insulation layer on first and second sidewalls of the multiple layer pattern;

forming a fourth conductive layer conforming to the first and second conductive sidewall spacers and the second gate insulation layer; and

removing a portion of the fourth conductive layer and the second gate insulation layer on the multiple layer pattern to expose the mask pattern and to leave portions of the conductive sidewall spacers and the fourth conductive layer remaining on the sidewalls of the tunnel junction barrier and adjacent portions of the second gate insulation layer.

33. A method according to Claim 32, wherein the conductive sidewall spacers and one or more semiconductor layers of the alternating semiconductor and tunnel insulation layers comprise silicon doped with impurities of a first conductivity type.

34. A method according to Claim 33, wherein the first conductive layer, the second conductive layer, and the fourth conductive layer comprise silicon doped with impurities of a second conductivity type.

35. A method according to Claim 32, wherein forming first and second impurity-doped regions in the substrate comprises implanting ions into the substrate using the portions of the conductive sidewall spacers and the fourth conductive layer remaining on the sidewalls of the tunnel junction barrier and adjacent portions of the second gate insulation layer as an implantation mask.

36. A method according to Claim 35, wherein forming a gate electrode further comprises recessing the remaining portions of the first and second conductive sidewall spacers and the fourth conductive layer thereon to below the mask pattern, and wherein the method further comprises:

forming a dielectric layer on the mask pattern and the recessed conductive sidewall spacers and fourth conductive layer;

planarizing the dielectric layer to expose the mask pattern;

removing portions of the mask pattern to expose the multiple layer pattern;

forming a fifth conductive layer on the substrate and in contact with the exposed multiple layer pattern; and

patterning the fifth conductive layer to form a data line.